Program of the 12th Prague Embedded Systems Workshop

Thursday, June 27

12:00-13:00	Lunch
13:00-13:20	Opening
13:20-14:20	**Keynote** - *Timo Kasper (Ruhr-University, Bochum, Germany; Kasper&Oswald GmbH.) and Tomáš Přeučil (FIT, CTU in Prague)* Colorful like a Chameleon: (In)Security of Wireless Access Control Systems Prediction
14:20-14:35	Coffee break
14:35-15:15	**Industrial Talk** - *Ondřej Holý (STMicroelectronics, Czech Rep.)* Progressive methods of driving permanent magnet synchronous motors (PMSM) with advanced algorithms and features
15:15-16:15 (2x 30)	**Session 1 – Architecture.** *Chair: Jiří Vyskočil*
	Jan Medek, Ondřej Golasowski and Michal Štěpanovský Single-cycle RISC-V processor microarchitecture design and implementation
	Oliver Haschke, Andreas Steininger and Florian Ferdinand Huemer Can Optimization Principles from Synchronous Adders be applied to Asynchronous (QDI) Ones?
16:15-16:30	Coffee break
16:30-17:30 (2x 30)	**Session 2 – Network Security.** *Chair: Tomáš Čejka*
	Lukáš Jančička, Josef Koumar, Dominik Soukup and Tomáš Čejka Analysis of Statistical Distribution Changes of Input Features in Network Traffic Classification Domain
	Dominik Soukup, Jaroslav Pešek, Lukáš Hejcman, David Beneš and Tomáš Čejka TCI: A system for distributed network monitoring, troubleshooting and dataset creation
???-18:30	Relax time
18:30-???	Dinner at the hotel restaurant + live music

Friday, June 28

10:00-11:00	**Keynote** - *Andreas Steininger (Vienna University of Technology, Austria)* Asynchronous Circuits – Old Iron or Enabler for a New Resilience Level of Digital Circuits?
11:00-11:15	Coffee break
11:15-12:15 (2x 30)	**Session 3 – Security 1.** *Chair: Vojtěch Miškovský*
	Philipp Schwind, Tobias Frauenschläger and Jürgen Mottok Implementation of a Bump-in-the-Wire Security Gateway
	Matúš Olekšák and Vojtěch Miškovský Effect of Compiler Optimization Flags on SipHash algorithm Side-Channel Information Leakage
12:15-12:40	**Industrial Talk** – *Martin Daněk (daiteq, Czech Rep.)*
12:40-14:00	Lunch + hanging posters
14:00-15:00	**Keynote** - *Jakub Šťastný (ASICentrum, s.r.o.)* Digital simulator: from the RTL to the full chip simulations of a low power SoC ASIC
15:00-15:40	**Industrial Talk** - *Milan Semmler (UJP Praha a.s., Czech Rep.)* The Czech Republic and Its Active Contribution to International Semiconductor Strategy Activities
15:40-16:10	**Poster session + coffee break**
16:10-16:40	**Industrial Talk** - *Marcus Pietzsch (Racyics GmbH., Germany)* Designing market ready energy efficient silicon in the first shot
16:40-17:00	Poster session evaluation
17:00-???	Social event - walking tour to Únětice brewery

Saturday, June 29

10:00-11:00	**Keynote** - *Virendra Singh (Indian Institute of Technology Bombay, Mumbai, India* Security Issues in Cyber Physical Cognitive Systems
11:00-11:15	Coffee break
11:15-12:45 (3x 30)	**Session 4 – Security 2.** *Chair: Stanislav Ježábek*
	Sacha Colucci and Jürgen Mottok Vulnerability Assessment of OPC UA Server Implementations
	Lukas Füreder and Jürgen Mottok Assessment of a MACsec-based Security System for Use in Critical Infrastructure Communication
	Ondřej Staníček, Filip Kodýtek and Róbert Lórencz Counter power leakage for frequency extraction of ring oscillators in ROPUF
12:45-13:00	Closing
13:00-???	Lunch