Alex Orailoğlu:

Alex Orailoglu received his S.B. Degree *cum laude* in applied mathematics from Harvard College, Cambridge, MA, and the M.S. and Ph.D. degrees in computer science from the University of Illinois at Urbana-Champaign, Urbana.

He is currently a Professor of Computer Science and Engineering with the Department of Computer Science and Engineering, University of California, San Diego, where he directs the Architecture, Reliability and Test (ART) Laboratory, focusing on VLSI test, computer architectures, reliability, embedded processors and systems, and nanoarchitectures. He has published more than 250 papers in these areas.

Dr. Orailoglu has served as the General Chair and the Program Chair for the *IEEE/ACM/IFIP International Symposium on Hardware/Software Codesign and System Synthesis*, the *IEEE VLSI Test Symposium*, the *IEEE Symposium on Application-Specific Processors (SASP)*, the *Symposium on Integrated Circuits and Systems Design (SBCCI)*, the *IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch)*, the *HiPEAC Workshop on Design for Reliability* and the *IEEE International High Level Design Validation and Test Workshop (HLDVT)*. He has last served as the *Program Co-Chair of IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) 2013*. He has co-founded the *IEEE SASP*, the *IEEE/ACM NanoArch*, the *IEEE HLDVT*, and the *HiPEAC Workshop on Design for Reliability*.

Professor Orailoglu has served as a member of the IEEE Test Technology Technical Council (TTTC) Executive Committee, as the Vice Chair of TTTC, as the Chair of the Test Technology Education Program group, as the Technical Activities Committee Chair and the Planning Co-Chair of TTTC and as the Communities Chair of the IEEE Computer Society Technical Activities Board. He is the founding chair of the IEEE Computer Society Task Force on Hardware/Software Codesign and the founding vice-chair of the IEEE Computer Society Technical Committee on NanoArchitectures.

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