Validating Power Management at Early Stages of Low-Power Systems Design

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Abstract

Power becomes a dominant problem in current hardware-systems design. It is usually dealt with use of power-management techniques, such as clock gating, power gating, or voltage scaling. In current complex systems, advanced power-reduction techniques are usually applied using some additional specification form, such as UPF (Unified Power Format) [1]. It enables a designer to introduce power-management aspects to the functional design, usually modelled in some HDL (Hardware Description Language). It was intended for RTL (Register-Transfer Level) and lower-level models. Although UPF has significantly helped designers to develop low-power systems, it is not suitable for modern design processes starting at the system level of abstraction. Therefore, new methods and methodologies have been developed to extend low-power design to the system level, such as [2,3]. Based on the analysis of their strengths and weaknesses, we have proposed a novel methodology for low-power systems design. It is specifically based on utilization of power management in specification stages and utilization of high-level synthesis to obtain a standard RTL model [4,5]. This short paper is focused on verification of the introduced power-management aspects at early stages of the design.

After the power management is specified, the specification has to be verified for functional and structural correctness and completeness. Since the model needs not be executable at early phases of design, a formal approach is suitable for this kind of verification. We use compilers to check syntactical correctness of the specification combined with the proposed static analysis revealing functional and structural inconsistencies of abstract power-management specification.

The next step is to verify the correct functionality of the low-power system. Since the abstract power-management specification does not model the effects on functionality, this verification step needs to be taken after the high-level synthesis process. Additional power-management elements are often a rich source of errors and must be verified for all specified operating modes. One of the advantages of the proposed methodology lies in the automation. Since the power-management specification at the RTL is automatically generated, we are able to avoid many power-related human errors issued during the power-management insertion at such a later stage. A designer does not need to worry about specifying the low-level power-management logic, such as power switches, isolation, retention, or level shifters. These are verified using the existing power-aware verification tools at the RTL.

To assure the power intent is preserved during the high-level synthesis, we propose the equivalence checking between the generated UPF specification and the abstract power management. The synthesized power-management unit is ideal for the assertion-based verification. The assertions are generated for verification of control sequences as well as for functional-coverage measurement.

In this way, the low-level power-related logic can be verified (both by simulation and formally) based only on the system-level abstract specification. This speeds-up the complex verification process (especially the preparation and debugging).

For evaluation of the proposed verification approach, we have used power-aware static analysis offered by Modelsim SE 10.2c. We have created several samples of abstract power-management specification and synthesized them into the UPF form. Modelsim successfully validated the generated UPF specifications; thus, the proposed verification steps indeed drive a designer to the correct power-management specification.

The abstraction and automated synthesis bring by themselves undeniable verification benefits. The abstraction results into very concise and intuitive specification, avoiding many common power-management errors. The early verification drives a designer to develop a complete and consistent power-management specification at the system level and the continuous verification steps during design flow ensure that the power intent stays preserved.

Paper origin

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