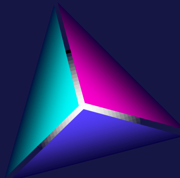

Towards Trusted Devices in FPGA by Modeling Radiation Induced Errors

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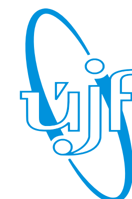
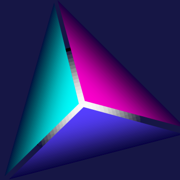




Problem definition

- FPGA
  - Programmable logic device
  - Lot of memory cells
    - Logic functions and interconnection - Configuration
    - D Flip-flops for sequential logic - Data

Hierarchy of FPGA interconnection

Switch blocks – global connections

LB

LB

LB

LB

LB

LB

Logic Block

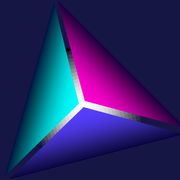
LUT

LUT

D

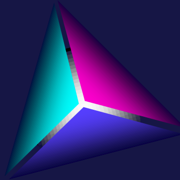
D

network



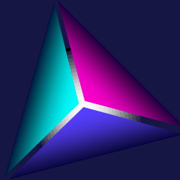
Problem definition

- FPGA
  - Programmable logic device
  - Lot of memory cells
    - Logic functions and interconnection - Configuration
    - D Flip-flops for sequential logic - Data
- CMOS
  - Small structures
  - Controlled by voltage
- Ionizing radiation
  - Transferring energy through matter
  - Depositing charge → inducing current → voltage change
- Problem: Single-event effects (SEE), mainly upsets (SEU)



SEU in FPGA

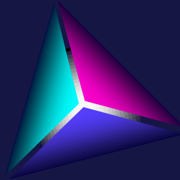
- Change of
  - Function (LUT)
  - Structure (interconnection)
  - Data (D-FF)
- Locally unpredictable – can hit any location
- Can influence dependability of the circuit/application
- But fightable by
  - Redundancy
  - Self check
  - Self repair (reconfiguration, ECC, …)
- Need of quantitative characteristic



Quantitative characteristic

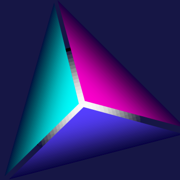
- Deep simulation to the level of CMOS technology
  - Unusable for real system – size
- Accelerated life testing (ALT)
  - Unusable for real system – too specific, too expensive
- Combination?
  - Partial simulation

    and
  - Partial ALT



Proposed Method

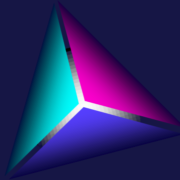
1. Create quantitatively described platform model
   a) Based on higher-level simulation
   b) Calibrated by Accelerated Life Tests
2. Use the model to predict any future design’s behavior on this platform



Proposed Method

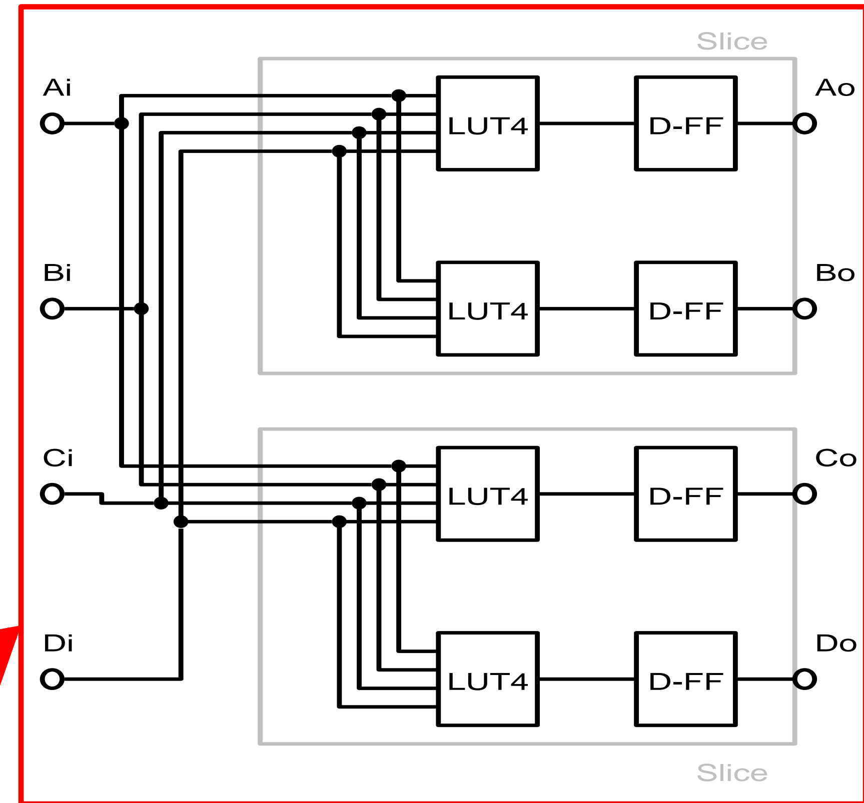
a) Higher-level simulation
- Based on VTR framework
  - Custom FPGA architecture
  - Timing-driven place-n-route on given platform
- Defect injection
- Fault simulation

a) Calibration by Accelerated Life Tests
- Only on several special designs
- Only for model calibration

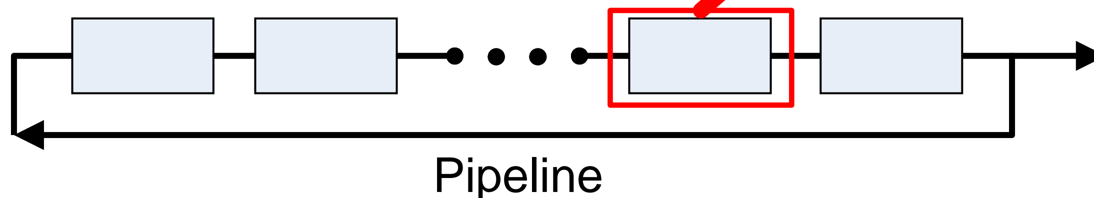


Test Circuit Example

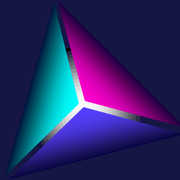
- Tests all LUTs and flip-flops
- Propagates any error to output
- Forms a long pipeline
- Is preloaded with data upon flip-flops reset
- Detects fault rate on the particular device under particular conditions



One pipeline stage



Pipeline

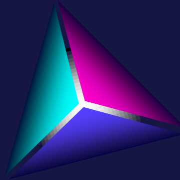


Test Circuit Example – Code

- Symmetric
- After odd number of conversions, the output is same as input
- Any bit flip in any LUT appears as a change in the sequence

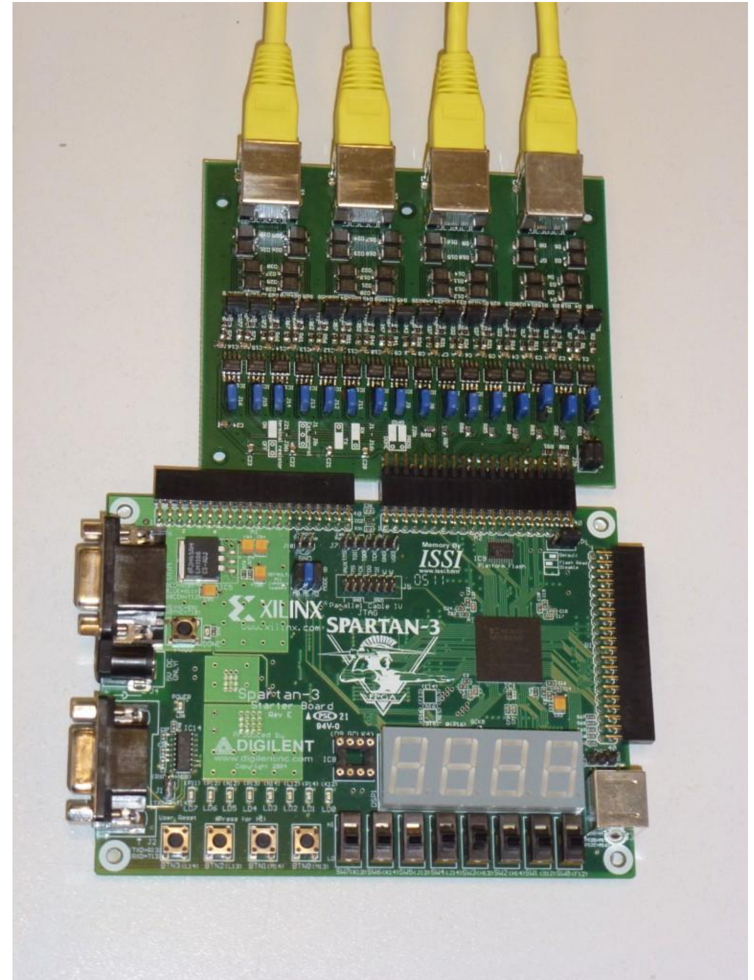
Code 1	Code 2
0000	1001
0001	1010
0010	1111
0011	0110
0100	0011
0101	0111
0110	1100
0111	0101

Code 1	Code 2
1000	1011
1001	0000
1010	0001
1011	1000
1100	0110
1101	1110
1110	1101
1111	0010



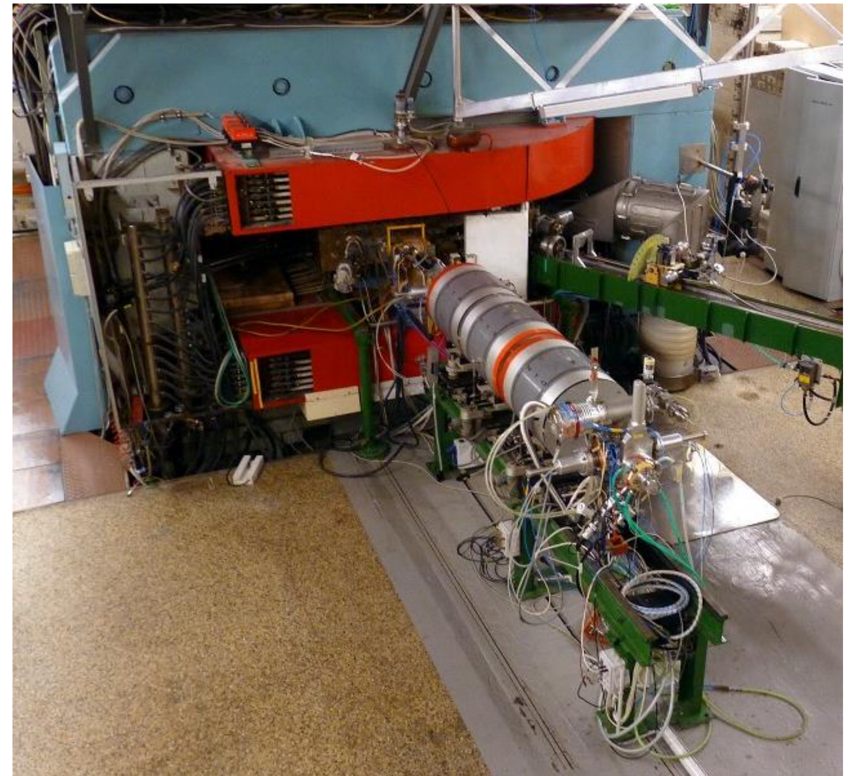
Entire Test System

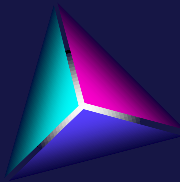
- Based on Spartan 3 Starter Kits
- Two parts
  - One under radiation
  - One away from radiation
- Connected trough 16 differential lines
- Radiated part is controlled from the shielded one
  - Remote monitoring, reset, reload



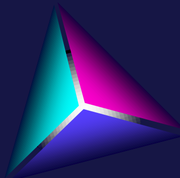
Cyclotron

- Isochronous cyclotron U-120M
- At NPI Řež, ASCR
- Up to 37 MeV protons
- Intensity from 10^4 p/cm^2/s

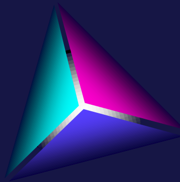




Irradiation Setup

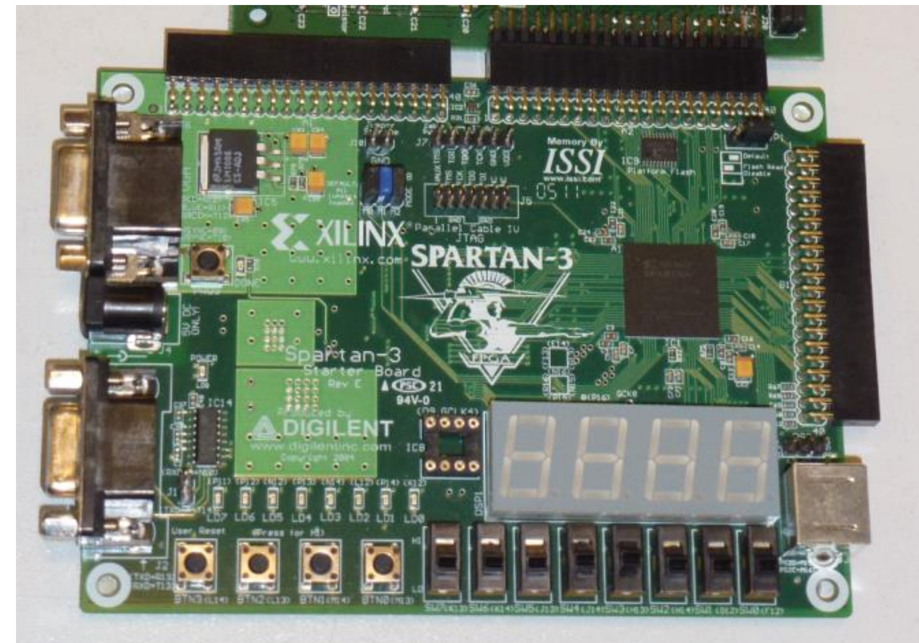


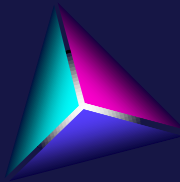
Irradiation Setup



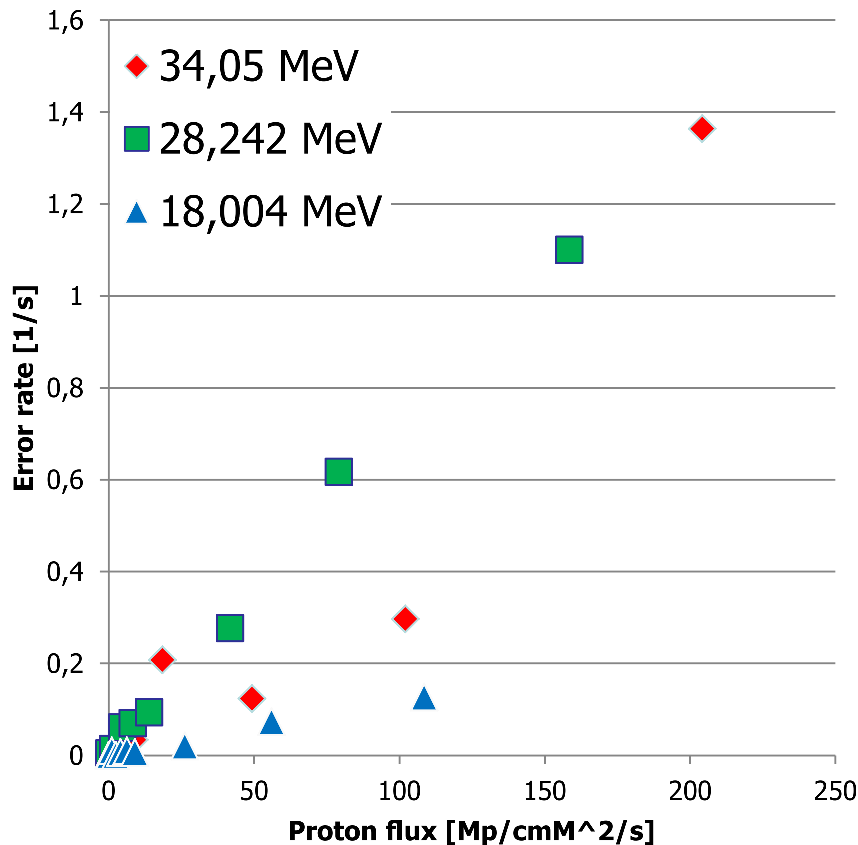
Spartan3 Irradiation

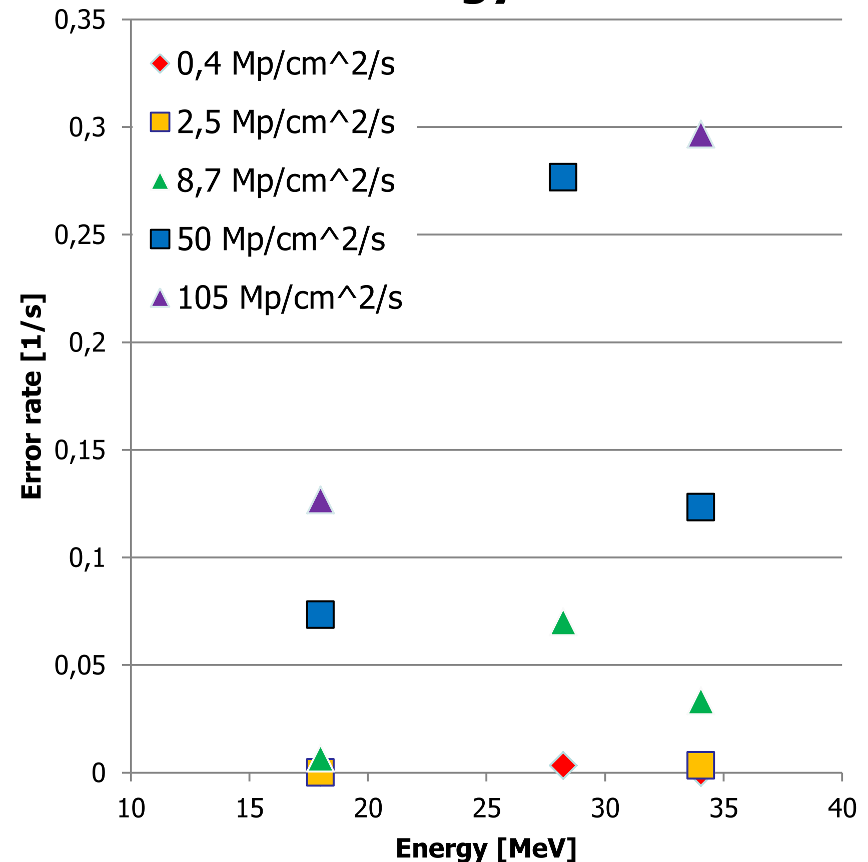
- Xilinx SRAM FPGA
- Starter Kit used
  - XC3S200 device
- 90 nm CMOS technology
- Only SEU in configuration memory (CMem) counted

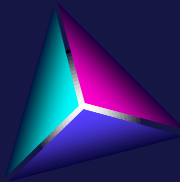




Spartan3 Irradiation

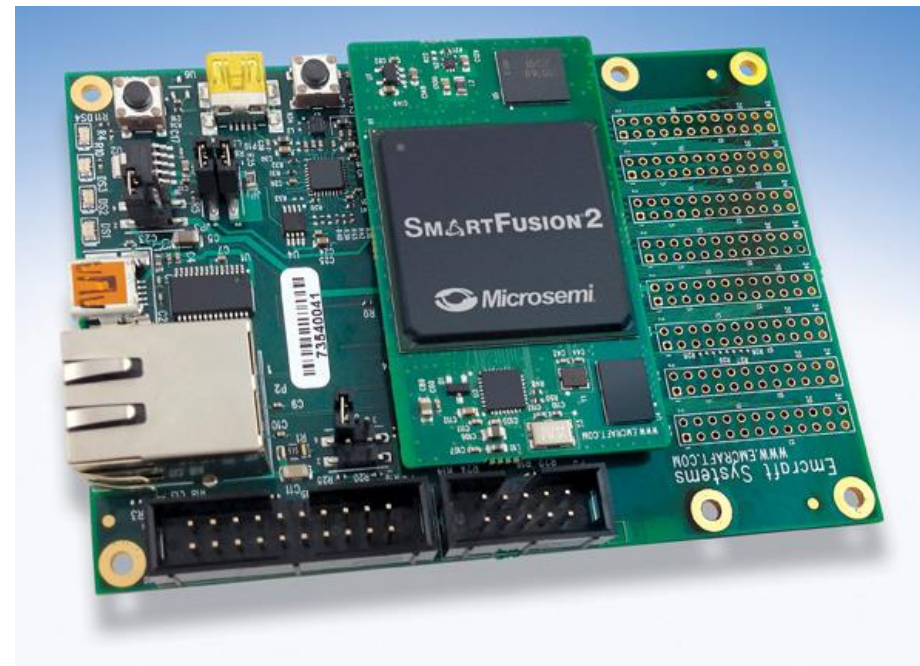


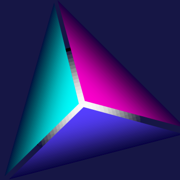




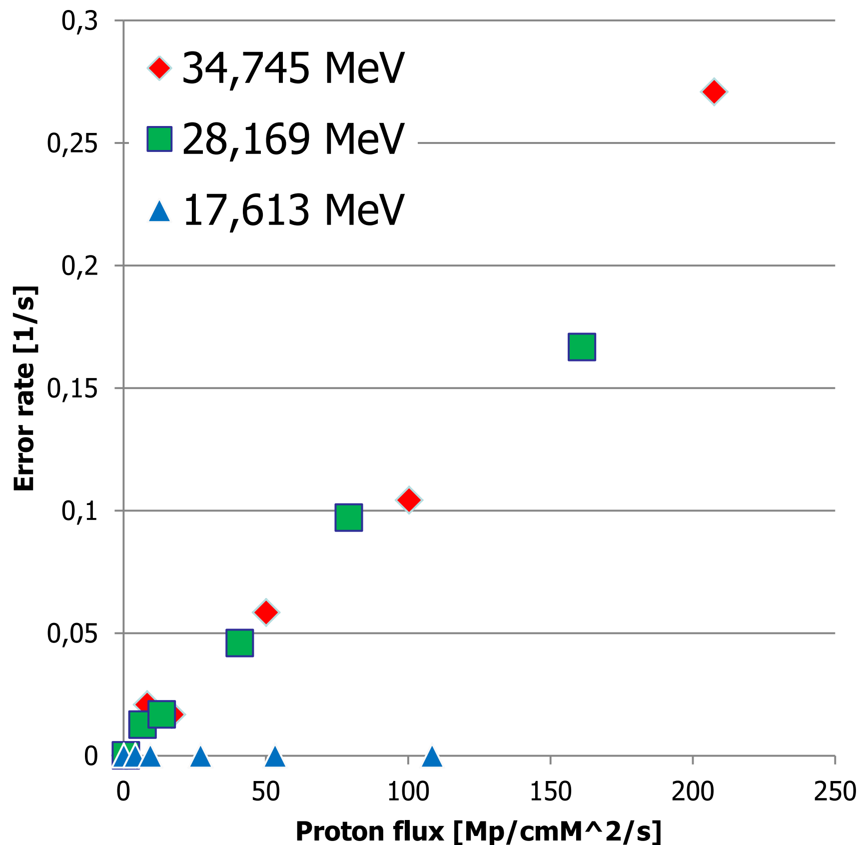
SmartFusion2 Irradiation

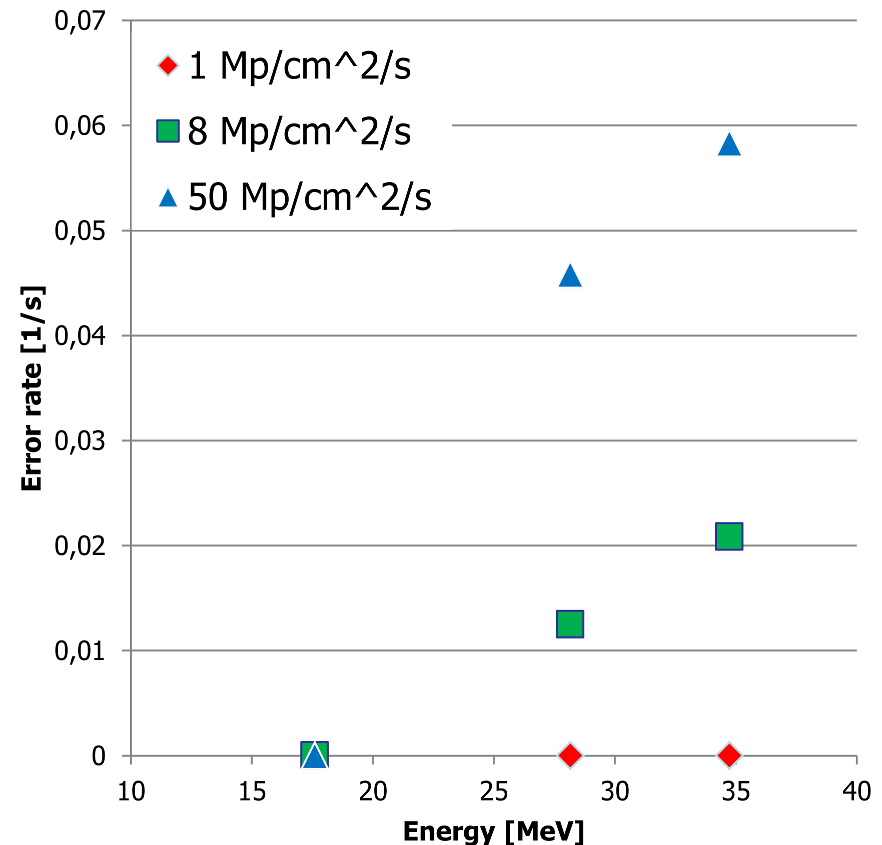
- Microsemi FLASH SoC
  - Only FPGA part tested
- Starter Kit used
  - M2S050-FGG484 device
- 65 nm CMOS technology
- No SEU in configuration memory
- Some SEU in “data” flip-flops (D-FFs)

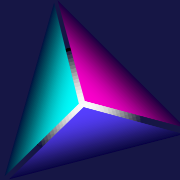




SmartFusion2 Irradiation

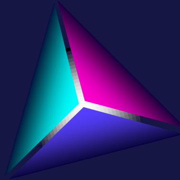






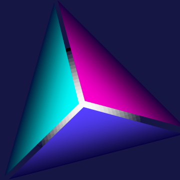
Current work

- Preparing the same test for the IGLOO2 FLASH based FPGA
- Precise monitoring of the total dose
- Upgrade the communication module
- Synchronization of the FPGAs clock with cyclotron frequency
- Improving model of architecture, collect another data and calibrate the model



Conclusions

- We have proposed **new method** for predicting quantitative characteristics of **SEU sensitivity** of **digital circuits** implemented in **FPGA**.
- We have completed the first runs of ALT.
- We are currently working on the simulation model, improving the ALT system and preparing the tests for other devices.
- This method can be used for verifying **dependability** and **security** parameters of various designs implemented in FPGA



Conclusions

- FLASH based SmartFusion 2 (65 nm) has better resistance to Single Event Effects than Spartan 3 (90 nm)
  - Configuration memory completely safe
  - D flip-flops less vulnerable, although it is a smaller technology
- But the SmartFusion 2 has a very low total ionizing dose to permanently destroy to destroy the FLASH programming controller.
  - ~4 kRads for SF2
  - Spartan 3 already survived several hundreds of kRads without permanent error noticed

Thank you!

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Special thanks to Jozef Ferencei

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