Proceedings (extended abstracts)

ESW 2013, 21-22 May, Temešvár, Czech Republic

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Programme

Tuesday May 21	13:30	ESW opening Presentations in Sessions **Dependability** • Hierarchical Dependability Models Based on Markov Chains • Self-Repair Modified Duplex System Architecture based on Reconfigurations **Theory** • XOR and Equivalence operators in Non-Exact Concept Learning	 Kohlík Borecký, Vít Rosensweig
	15:30	Coffee break	
	16:00	**Applications** • Applications of digital systems • New Approaches to a Connection of Memory Consistency and Cache Coherence • Hardware Support For Precise Time and Frequency Distribution **Faults in FPGA** • FPGA bitstream SEU effect emulation and evaluation • A New Method of Modeling Radiation-Induced Soft Errors in FPGA by Architecture Analysis	Mróz, Zając, Pławiak-Mowna Kašpar Dostál Kvasnička Pospíšil, Vaňát
	18.30	Dinner	
	20.00	PC meeting	

Wednesday May 22			
	8.00	Breakfast	
	9.00	**Networking** • Real-time Network Measurement for High-Speed Networks • Real-time Detection of Anomalies in High-speed Computer Networks • The Behavior Network (BeNet) **Testing** • Test Pattern Decompression in Parallel Scan Chain Architecture	Benáček Čejka Šlechta Chloupek
	12.00	Lunch	
	13:30	Closing discussion	

Dependability

- **Hierarchical Dependability Models Based on Markov Chains**. Martin Kohlík, FIT.
  Abstract
  Dependability models allow calculating the rate of an event leading to a hazard state - a situation, where safety of the modeled dependable system (e.g. railway station signaling and interlocking equipment, automotive systems, etc.) is violated, thus the system may cause material loss, serious injuries or casualties. A hierarchical dependability model based on Markov chains allows expressing multiple redundancies made at multiple levels of a system decomposed to multiple cooperating blocks by Markov chains. The hierarchical model utilize decomposition, thus a complex dependability model is divided into multiple small models. The decomposed model is easier to read, understand and modify. The hazard rate is calculated significantly faster using hierarchical model, because the decomposition allows exponential calculation-time explosion to be avoided. The paper shows a method of reducing Markov chains and using them to create hierarchical dependability models. Two example studies are used to demonstrate the advantages of the hierarchical dependability models.

- **Self-Repair Modified Duplex System Architecture based on Reconfigurations**. Jaroslav Borecký, Pavel Vít, FIT
  Abstract
  This paper describes our aims, how to increase dependability parameters (safety and reliability) of a system based on programmable hardware (FPGAs) against transient faults like a Single Event Upset. We combine Concurrent Error Detection (CED) techniques, FPGA reconfigurations and our Modified Duplex System (MDS) architecture. Our new methodology is developed for industrial practical FPGA applications and is proposed to reach the minimal area overhead for the possible future low-power SoC (System on a chip) design. It is aimed especially for modular systems. The method uses static and partial dynamic reconfiguration of FGPAs where a design is decomposed into totally self-checking blocks. The type and size of blocks to reconfigure depends on the used architecture and on the particular construction of a secured sytem.

Theory

- **XOR and Equivalence operators in Non-Exact Concept Learning**. Hillel Rosensweig and Ilya Levin
  Abstract
  Often, Learning includes examining a group of objects, and formalizing a description - a concept - based on shared characteristics. Concepts are the atoms of thought and are at the nucleus of cognition science. People acquire concepts from infancy and continue throughout their entire lives by utilizing existing concepts in complex combinations.
  One significant class of Concepts is Boolean concepts (Boolean Concept Learning - BCL). Boolean concepts have the form of Boolean functions, with Variables which may be defined in non-Boolean terms (for instance - the concept of legality has two possible values (legal\illegal), but is defined by context and variables which are not, in themselves, Boolean).

One area of interest is the Subjective concept complexity – a measurement of the difficulty of learning a specific Boolean Concept. Finding a measurement of cognitive complexity is closely linked to the question of the mechanism of concept learning. Existing research relates concept complexity to factors such as: minimum Boolean function representation (Feldman, 2000), spectral density of Boolean functions in the implication plane (Feldman 2006), functional invariance (Vigo, 2009), and cognitive representation(Johnson-Laird, 2011).
A novel approach to understanding subjective concept complexity and Concept Learning views Concepts learning as a non-exact process, where people make approximations of complex systems in order to function around them (Levin, Keren & Rosensweig, 2012). According to this approach, there is a complex and intelligent mechanism at work in the manner in which people approximate a Boolean concept. This approach tries to understand the mechanism of Non Exact learning, and to trace back learned concepts to their Boolean Functional properties – properties recognized from the algebraic and engineering study of Boolean Functions (such as Linearity, Symmetry, etc.).
In a BCL study conducted, 137 subjects were given a series of Bongard Problems to solve. Bongard Problems are a set of 100 problems created by M. M. Bongard. Each problem presents two sets of relatively simple diagrams, BP_left and BP_right. All the diagrams from BP_left have a common characteristic, which does not exist in the images of BP_right. The problem is to find and formulate a convincing distinction rule between both sides.
Bongard problems are, generally, well suited for examining formation of a Boolean Concept. We view solutions - distinction rules - created by subjects as Boolean functions classifying the characteristics of BP_left and BP_right.
In this study, all subject solutions to a Bongard Problem are compared to possible correct solutions and to solutions by other subjects. Our results indicate that Equivalence and XOR operators are of unique importance in Human concept learning. In other words, a key process in Non-Exact modeling is finding XOR or Equivalence relations between variables, as a basis for more complex concept creation.

Applications

- **Applications of digital systems.** Piotr Mróz, Wojciech Zając and Anna Pławiak-Mowna
  Abstract

- **New Approaches to a Connection of Memory Consistency and Cache Coherence.** Jiří Kašpar.
  Abstract
  The correctness of shared memory operations in modern multi-core and multiprocessor systems depends on the memory consistency model and the cache coherence. An evolution of consistency models was mostly driven by requirement of expected behavior in case of increasing instruction parallelism and asynchronous memory accesses from any core. The cache coherence provides a speedup of memory operations with no functional change. All mainstream multi-core CPUs support the consistency model using an enhanced variant of the MESI

cache coherency protocol based on the single-writer–multiple-reader (SWMR) invariant. To enable faster execution, we studied parallel algorithms with respect to the SWMR invariant. Our result describes a new classification of shared memory access patterns with several new classes. We analyze their impact on an ISA, a compiler and an operating system. A model of proposed architecture in GEM5 emulator is currently under development.

- **Hardware Support For Precise Time and Frequency Distribution.** Jiří Dostál
  Abstract
  The extended abstract describes methods of time interval measurement which are suitable for FPGA implementation. There are further described the applications of the precise time and frequency distribution: the IEEE 1588 timestamper and the FPGA based time measurement device.
  A New Method of Modeling Radiation-Induced Soft Errors in FPGA by Architecture Analysis

Faults in FPGA

- **FPGA bitstream SEU effect emulation and evaluation.** Jiří Kvasnička
  Abstract
  The presentation will show the effect of bitstream single-bit malfunction in the FPGA. The primary motivation of this study is an evaluation of the SEU susceptibility of the real design, that is placed and routed in the FPGA. Two methods of how to evaluate the effect will be described.
  First method use a hardware emulator, that observes the effect directly in the FPGA. It emulates the bitstream SEU by a FPGA bitstream bit manipulation, which is performed by a dynamic reconfiguration. Every single bit of the bitstream is altered and effect evaluated by output comparison with golden (unmodified) copy of the test circuit. The platform for the hardware emulator is Atmel FPSLIC, which controls both the reconfiguration and testing from within the chip. The test designs for the hardware emulator can also contain the basic error detection circuit, the parity predictor.
  Second method predicts the effect directly from the bitstream file, assuming the FPGA structure and bitstream structure is understood. The prediction stands on simple fault models, but the FPGA structure knowledge is the key problem to overcome. Unless the structure is provided by the FPGA vendor, the bitstream has to be reverse engineered. Overview of the effect prediction and the bitstream analysis (reverse engineering) will be given for the Atmel FPSLIC FPGA device. The summary and comparison of both method results will be given, showing the number of vulnerable bits in the various-sized designs and same designs incorporating parity predictor.

- **A New Method of Modeling Radiation-Induced Soft Errors in FPGA by Architecture Analysis**. Jan Pospíšil, Tomáš Vaňát
  Abstract
  Recently, FPGA devices are more often used in applications demanding dependability and safety. These FPGAs are, nevertheless, manufactured using CMOS technology with SRAM memory cells, which are prone to ionizing radiation. In our work we propose a method of modeling the behavior of FPGA in radiation

harsh environment based on parameters obtained from experiments on real hardware. The proposed method utilizes academic toolchain VPR. By modifications of this toolchain, and from SEU characteristics gathered from "in vivo" experiments, a modeling and simulation platform for future designs can be constructed, with close-to-reality results.

Networking

- **Real-time Network Measurement for High-Speed Networks**. Pavel Benáček
  Abstract
  The main goal of this presentation is to introduce an alternative way of high-speed network monitoring device implementation. The main goal of my work is to provide formalism and usable tool for monitoring system generated from HLL (high-level language) description to support network speeds above 40 Gbps. The main problem we need to deal with is to define a general description of measurement process which could be used for subsequent transformations (to HDL for use in FPGA/ASIC for example).

- **Real-time Detection of Anomalies in High-speed Computer Networks**. Tomáš Čejka
  Abstract
  This paper deals with a method for detection of anomalies (e.g. attacks) in high-speed computer networks in real-time — with minimal delay while the false alarm rate is controlled at a prescribed low level. In addition, our vision is to create a monitoring system that can dynamically adapt its parameters to change its focus on more detailed information about traffic relevant to the anomaly. It will be able to dynamically increase the frequency of sampling in a subset of the observed network traffic characteristics, and start storing more information for forensic analysis. The detection delays of the method are minimized using non-parametric sequential change-point detection. The system then precisely localizes anomalies via comparison of single line and "Broken-stick" linear models. The target of the method is detection in high-speed computer networks working at 100 Gbps speeds. With the proposed real-time detection method the system has a promise for timely reconfiguration and more sophisticated analysis of and reactions to attacks even in ultra high-speed networks. As a proof of concept, we are currently developing the detection system using the COMBOL-1G4 card. The card is equipped with four 1 Gbps Ethernet interfaces and a VIRTEX 5 FPGA chip. We use two interfaces for monitoring and/or forwarding the traffic, and other two for management and transmission of calculated aggregate values of the observed characteristics. The two monitoring ports can be configured either as a wire-tap, or to monitor two different Ethernet lines terminated in the COMBOL card.
  Usage of the card interfaces is shown in Fig. 1. The card is deployed as a stand-alone monitoring probe. It is pre-loaded with our hardware design that currently counts the numbers of packets of specific types. The aggregate values (currently packet counts) from one or more probes are used as input for the detection method that is deployed on a remote detection machine. The detection system consisting of this hardware card and software will be deployed and tested on our faculty network to detect anomalies.

- **The Behavior Network (BeNet).** Jan Šlechta
  Abstract
  The Behavior Network concept and structure is presented. As the example a controller behavior is designed. Both the system decomposition of finite state machines and the mission oriented view are described.

Testing

- **Test Pattern Decompression in Parallel Scan Chain Architecture**. Martin Chloupek
  Abstract
  The paper presents a test-data volume-compression method which reduces test time and hardware overhead by test pattern broadcast into parallel scan chains. The proposed hardware enables efficient test pattern decompression and test response compaction. It uses a XOR-less structure instead of ring generators for test pattern decompression. Decompressed test vectors are obtained from the previously generated ones by simple shift operations only. The compression algorithm can search in a wider pattern space when finding the best fitting decompressor seed sequence because of this arrangement. The faults of basic gates can be covered by the patterns easily obtained in the decompressor during several clock cycles as a majority of faults can be tested by patterns that differ in a few shift operations only. The paper describes a test pattern decompressor hardware including its controller. The decompressor reduces the number of flip-flops containing information about previously generated pattern by test pattern broadcast into parallel scan chains. The memory requirements, test time and hardware overhead are compared with the parameters of circuits designed by the industrial test compression and compaction tools. The hardware realization can be modified according the required tradeoff between the complexity of test sequence control and the hardware overhead.