Hardware Support For Precise Time and Frequency Distribution

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1 Introduction to precise time and frequency distribution

The need for precise time and frequency synchronization between devices with microsecond accuracy is nowadays not only scietific problem but it has much more practical impact. Precise time is of course the base of the GPS system and modern telecomunications. There are also new fields of precise time application e.g. finance and high frequency trading. Therefore is important somehow to distribute the precise time practically – the easiest way to do this is utilizing existing computer networks.

2 IEEE 1588 timestamper

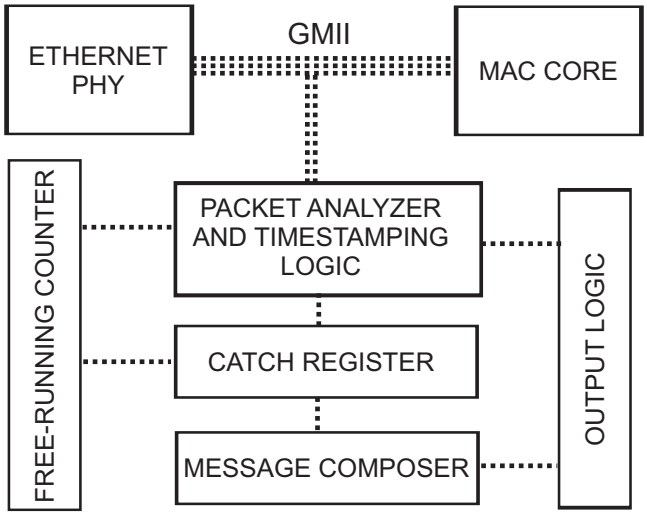

Figure 1: Simplified block diagram of the IEEE 1588 timestamper. The packet analyzer and packet logic is implemented as FSM. Free-runnig counter on reference frequency is timestamped by the start of frame delimiter event. If the PTP message match the configurable criteria the message with timestamp is composed and is sent to the higher PTP logic via output logic.

IEEE 1588 is a relatively new protocol standard for a precision clok synchronization. It operates mostly over TCP/IP networks and Ethernet. The protocol is also known as the Precision Time Protocol – PTP. Synchronization architecture is a master–slave model with nodes comunicating primary by multicast. The main difference between PTP and its predecessor NTP is that the PTP enabled nodes have to be equipped by some HW support to precise the delay measurement. You can find more about this protocol in [1].

The IEEE 1588 is a device which creates timestamps of incoming/outcoming packets in network interface hardware and the timestamp is further used in the PTP functionality. The timestamper is placed between the PHY and MAC layer on a MII interface and listen to the traffic. Every PTP packet is timestamped so if there is a lag in the network hardware between the composition and sending, we will know the correct time of physical transmission of the packet. The correct timestamp of a Sync message is sent as a Follow up message.

The timestamper is implemented as IP core for FPGA in VHDL language and the simplified block diagram is in figure 1. The timestamping core is configurable and can operate on Layer 2, 3 and 4 of the ISO/OSI model and also the reference frequency of the free-running counter.

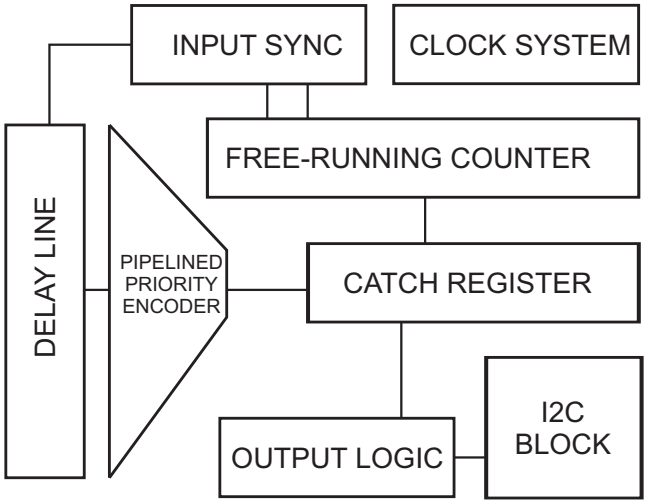

Figure 2: Simplified block diagram of the FPGA counter with carry chain interpolation. There are couarse free-runnig counter driven by reference frequency. The intervals within one clock period is measured by the tapped delay line interpolator (carry chain implementation). The propagation rate of delay line is computed in the pipelined priority encoder. Measured values are stored in the catch registers and sent by the output logic. The I2C block reads service information from transceivers and manage the frequency synthesis on the daughter card.

3 Time interval measurement methods suitable for FPGA designs

3.1 Coarse time interval measurement

Coarse time interval measurement is the fundamental method. In this method we have the incremental counter which is driven by the refernce clock with frequency f_{ref} with the appropriate period $T_{ref} = 1/f_{ref}$ – this is also the resolution. The coarse measurement is simply done by sampling the incremental counter by the START and STOP events which determines the duration of the measured time interval. The samples are two integer nubmers n_{START} and n_{STOP} hence the nuber of periods is $n = n_{STOP} - n_{START}$ and the resul of the coarse time interval measurement is equal to $n \cdot T_{ref}$. START and STOP signals are asynchronous to the f_{ref} time domain so the maximum quantization error of single measurement is $\pm T_{ref}$. For the more precise (less then T_{ref}) measurement we have to use some of interpolation methods.

3.2 Tapped delay line method

Tapped delay line method is based on sampling the propagation of START event in the delay line. The delay line is composed of serial connected delay elements with delay τ and the each output of the delay element is connected to a D flip-flop. All of the flip-flops creates a catch register which is driven by the STOP signal. The delay line is feeded by the START signal which after the START event propagates trough the delay elements. After the STOP event the state of the delay is sampled into the catch register as a series of ones and zeros. If the number of ones is n_{ones} we can calculate the value of time interval between the START and STOP events as $n_{ones} \cdot \tau$.

3.3 Vernier interpolator

In this method there are two delay lines DL_1 and DL_2 consisted with delay elements with slightly different delay τ_1 and τ_2. Delay elements outputs are conected to a catch register (D flip-flops), delay line 1 is conected to the data inputs and delay line 2 to the clock inputs of the individual D flip-flop. Delay line 1 is feeded by START signal while delay line 2 is feede by STOP signal. The result is stored in the catch register and then is decoded to the corresponding time value.

3.4 Comparison

For implementation in FPGA are suitable both methods but the *Vernier method is slightly more complex* than the tapped delay line. It is difficult to implement two delay lines with similar delay propagation in the FPGA technology. The catch D flip-flops also have to be manually placed into correct position. An *implementation of*

the tapped delay line in FPGA is much more easier. We can with advantage utilize carry chain entities which have regular structure and are connected physically to a one row so the delay propagation is uniform.

4 FPGA based time measurement device

The device is based on the Virtex-5 FPGA board with custom-designed daughter card with DWDM transcievers and frequency synthesis functionality. The simplified block diagram is in figure 2.Pair of these devices acts as PPS transceiver and can propagate and measure performance of reference clocks remotely over DWDM network for distances about hundreds of kilometers.

References

[1] IEEE standard for a precision clock synchronization protocol for networked measurement and control systems. New York, 2008. ISBN 978-073-8154-008.

[2] Loffredo, S. Design, construction and tests of a high resolution, high dynamic range Time to Digital Converter. Roma, 2010. Universita degli studi Roma Tre.

[3] Pedersen, K. Low cost, high performance frequency/interval counters. 2008.

[4] Kalisz, J., Szplet, R. A PC-based time interval counter with 200 ps resolution. Warsaw, 2003. Military University of Technology.

[5] Favi, C., Carbon, E. A 17 ps Time-to-Digital Converter Implemented in 65nm FPGA Technology. Lausanne, 2009. École Polytechnique Fédérale de Lausanne.

[6] Dostál, J. Přenos času a frekvence v lokálních sítích. PAD 2012, pp. 43-48. ISBN 978-80-01-05106-1.