Test Pattern Decompression in Parallel Scan Chain Architecture

Martin Chloupek

Czech Technical University in Prague
Thakurova 9, Prague, Czech Republic
Martin.Chloupek@fit.cvut.cz

Abstract. The paper presents a test-data volume-compression method which reduces test time and hardware overhead by test pattern broadcast into parallel scan chains. The proposed hardware enables efficient test pattern decompression and test response compaction. It uses a XOR-less structure instead of ring generators for test pattern decompression. Decompressed test vectors are obtained from the previously generated ones by simple shift operations only. The compression algorithm can search in a wider pattern space when finding the best fitting decompressor seed sequence because of this arrangement. The faults of basic gates can be covered by the patterns easily obtained in the decompressor during several clock cycles as a majority of faults can be tested by patterns that differ in a few shift operations only. The paper describes a test pattern decompressor hardware including its controller. The decompressor reduces the number of flip-flops containing information about previously generated pattern by test pattern broadcast into parallel scan chains. The memory requirements, test time and hardware overhead are compared with the parameters of circuits designed by the industrial test compression and compaction tools. The hardware realization can be modified according the required tradeoff between the complexity of test sequence control and the hardware overhead. This research has been published in [1].

References

1. Chloupek, M., Jenicek, J., Novak, O., Rozkovec, R.: Test Pattern Decompression in Parallel Scan Chain Architecture. In IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), April 2013.

This research has been partially supported by the grant of the Czech Technical University in Prague No. SGS12/094/OHK3/1T/18.